WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:

a plurality of internal circuits for generating a plurality of internal signals, the internal signals used for addressing storage locations and for controlling internal operations;

a selection circuit for controlling transfer paths of the internal signals and data in response to selection signals, the selection signals corresponding to test information signals; and

a data output buffer for transferring the internal signals to an outside of the device through data input/output pads.

2. An integrated circuit device comprising:

a plurality of internal circuits for generating a plurality of internal signals, the internal signals used for addressing storage locations and for controlling internal operations;

a first selection circuit for receiving the internal circuits in response to selection signals corresponding to test information signals;

a second selection circuit for receiving output signals from the first selection circuit and output signals from a sense amplifier, and for opening an alternative one of transfer paths of the internal signals and the output signals in response to the selection signals; and

a data output buffer for transferring output signals from the second selection signals to an outside of the device through data input/output pads.

3. A method for monitoring internal signals in an integrated circuit device having input/output pads, the method comprising the steps of:

detecting a test mode;

selecting a part of internal signals of the integrated circuit device; and

transferring the part of the internal signals to an outside of the integrated circuit device through the input/output pads.

4. A method for monitoring internal signals in an integrated circuit device having sense amplifier, a data output buffer, and input/output pads, the method comprising the steps of:

detecting a test mode in response to a logical states with external control signals of the integrated circuit device;

selecting a part of internal signals of the integrated circuit device in response to selection signals corresponding to test information signals;

selecting an alternative one of transfer paths of the part of the internal signals and output signals from the sense amplifier in response to the selection signals; and

transferring the part of the internal signals to an outside of the integrated circuit device through the data output buffer and the input/output pads.